REMARKS

Claims 1-4 and 7-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamiya, *et al.* (U.S. patent number 6,080,624) taken with what is referred to as the applicant admitted prior art (APA) in the specification at page 1 line 16 through page 3 line 20 and Figures 1, 2A-2B, and Kamiya, *et al.* (U.S. patent no. 5,838,615). Claims 1-4, 6-10 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the APA taken with Kamiya, *et al.* '624 and Kamiya , *et al.* '615. Claims 5 and 11 are rejected under 35 U.S.C § 103(a) as being unpatentable over Kamiya, *et al.* '624 and the APA, or vice versa, and Kamiya, *et al.* '615 and further in view of Ma, *et al.* (U.S. patent number 5,280,446) or Fazan, *et al.* (U.S. patent number 6,066,528). In view of the amendments to the claims in the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

Referring, for example, to Figures 3A and 4A of the present application and the specification at page 8 line 15 through page 10 line 15, the applicants' invention is directed to a method of fabricating a NAND-type flash memory device. The applicants' device includes an array of memory cells C1 through Cn, which are contacted in one direction by word lines WL1 through WLn and in the perpendicular direction by bit lines 55. The array is configured as a group of strings. Each string includes a string select transistor SST and a ground select transistor GST, with the cell transistors C of the string being disposed serially between the string select transistor and the ground select transistor. The strings are disposed adjacent to each other, and each string runs from string select transistor SST through the cell transistors C of the string to the ground select transistor GST of the string, in the direction of the bit lines 55.

In the direction of the word lines WL, the array includes a string selection line SSL, which runs across the string selection transistors, a ground selection line GSL, which runs across the ground select transistors and word lines WL1 through WLn which run across the cell transistors. A common source line 48 runs in parallel with and in the same direction as the word lines, the string selection line and the ground selection line. The common source line is connected to the source regions of the ground select transistors GST. The Examiner is referred in

particular to the specification at page 8 lines 28 through 29 and page 10 lines 11 through 12, wherein it is stated that the applicants' common source line 48 is connected to sources of the ground select transistors GST and that the bit lines 55 cross over the word lines and the common source line 48. That is, the common source line of the invention runs in parallel to the word lines, and both the word lines and the common source line run in a direction perpendicular to the bit lines.

These features of the applicants' invention are clearly set forth in the amended claims. The claims clearly state that the string selection line pattern, the ground selection line pattern and the word lines are all formed to be in parallel with each other. The claims also state that source regions are formed adjacent to the ground selection line pattern. The claims also state that the common source line is formed on the source regions, that the common source line runs parallel with the ground selection line pattern and is electrically connected to the source regions.

These features of the invention are neither taught nor suggested by any of the cited prior art references, taken alone or in combination.

Kamiya, *et al.* ('624) teaches a memory device that is fabricated in a way that is very different from the applicants' claimed method. Specifically, referring to Figure 3, for example, of Kamiya, *et al.* ('624), the Kamiya, *et al.* ('624) memory device includes a memory cell group 100, which includes cell transistors 101. The cell transistors 101 are connected to source lines 131, which are disposed in parallel to bit lines 133 and perpendicular to word lines 132. A contact portion 121 referred to by the Examiner as the applicants' claimed common source line, connects the cell transistors 101 to vertical source lines 131. That is, the source of each cell transistor 101 is connected to a source line 131 via a contact portion 121.

This manner of forming a memory circuit disclosed in Kamiya, *et al.* is very different from the applicants' claimed approach. For example, notwithstanding the Examiner's reference to contact portion 121 as the claimed common source line, the Kamiya, *et al.* ('624) patent explicitly teaches that its source line is line 131, which is parallel to bit lines 133, not crossing over the bit lines, as the applicants claim. Furthermore, neither the Kamiya, *et al.* ('624) source

line 131 nor the Kamiya, *et al.* ('624) contact portions 121 are connected to active source regions along a ground selection line pattern, as claimed by the applicants. Instead, Kamiya, *et al.* ('624) explicitly teach that the contact portions 121 are connected to sources of the cell transistors, and the source line 131 is connected to the contact portions, not to any source regions at all. There is no disclosure of ground select transistors in Kamiya, *et al.* ('624), and, even if there were, the Kamiya, *et al.* ('624) patent explicitly states that the contact portions 121 are connected to cell transistors 101 (See Kamiya, *et al.* ('624) at column 5, lines 48-54). In contrast, in the applicants' claimed invention, the common source line is connected to sources of ground select transistors, not to the cell transistors C.

Although the Examiner refers to Kamiya, *et al.* ('624) as teaching a string selection line pattern, a plurality of word line patterns and a line pattern (presumably the applicants' claimed ground selection line pattern) crossing over isolation layers and active regions, the applicants have studied the entire Kamiya, *et al.* ('624) reference and have been able to find no such teaching. That is, there is no teaching or suggestion in Kamiya, *et al.* ('624) of the applicants' claimed string selection line pattern or the applicants' claimed ground selection line pattern. If the Examiner disagrees with the applicants' interpretation of the reference, it is respectfully requested that the Examiner specifically refer to these features in the Kamiya, *et al.* ('624) patent, perhaps by reference numeral and/or by column and line number.

The Examiner also refers to contact holes 130a of Kamiya, *et al.* as the slit-type common source line contact hole of the claimed invention. As disclosed in Kamiya, *et al.* ('624) at column 8 lines 16 through 19, the contact holes 130a are filled with a tungsten film 151 to form the contact portions 121 communicating with the source diffusion layers of the cell transistors 101. The contact holes 130a of Kamiya, *et al.* ('624) are not the applicants' claimed slit-type common source line contact hole, because the slit-type common source line contact hole of the applicants' claimed invention is used to form the applicants' claimed common source line which is connected to source regions along a ground selection line pattern and, as noted above, Kamiya, *et al.* ('624) neither teach nor suggests a ground selection line pattern and, as noted above, the

contact portion 121 of Kamiya, *et al.* ('624) is not the applicants' claimed common source line.

The APA set forth in the applicants' specification also fails to teach or suggest the applicants' claimed slit-type common source line contact hole used in forming the common source region of the claimed invention.

Kamiya, *et al.* ('615) also fails to teach or suggest features of the invention set forth in the amended claims. Specifically, Kamiya, *et al.* ('615) fails to teach or suggest the applicants' claimed common source line connected to sources along a ground selection line pattern. Kamiya, *et al.* ('615), like Kamiya, *et al.* ('624), does not teach or suggest a string selection line pattern or a ground selection line pattern running along a plurality of word line patterns, as set forth in the amended claims. Likewise, Kamiya, *et al.* ('615) also fails to teach or suggest a common source line connected to source regions along the ground selection line pattern and running parallel to the string selection line pattern, the ground selection pattern and the word lines. Referring to Kamiya, *et al.* ('615) at column 5 lines 4 through 39, and Figures 2-4, a slit-like opening 114 is formed on a source diffusion layer 109 between two adjacent memory cell transistors 105. A tungsten film 115 is formed in the slit 114. The tungsten film 115 is connected to a diffusion layer 109 of cell transistors 105. Once again, the tungsten film 115 of Kamiya, *et al.* ('615) is not the applicants' claimed common source line. That is, the tungsten film 115 is not a slit-type common source line connected to source regions along a ground selection line pattern, as set forth in the amended claims.

None of the three cited references, namely, Kamiya, *et al.* ('624), the APA and Kamiya, *et al.* ('615), teaches or suggests the invention set forth in the amended claims. Specifically, none of the references teaches or suggests the applicants' claimed common source line in a slit-like common source line contact hole which runs in the same direction as a string selection line pattern, a plurality of word line patterns and a ground selection line pattern and is connected to source regions disposed along the ground selection line pattern. Since none of the cited references teach this feature of the invention, there is no combination of the references which would provide such teaching or suggestion.

None of the references, taken alone or in combination, teach or suggest the invention set forth in the amended claims. Accordingly, it is believed that the amended claims are allowable over the cited references. Accordingly, reconsideration of the rejections of claims 1-4 and 7-10 under 35 U.S.C. §103(a) as being unpatentable over Kamiya, *et al.* ('624), taken with the APA and Kamiya, *et al.* ('615) is respectfully requested. Likewise, reconsideration of the rejections of claims 1-4, 6-10 and 12 under 35 U.S.C. §103(a) as being unpatentable over the APA taken with Kamiya, *et al.* ('624) and Kamiya, *et al.* ('615) is respectfully requested.

With regard to the rejections of claims 5 and 11, neither of Ma, *et al.* (U.S. Patent Number 5,280,446) and Fazan, *et al.* (U.S. Patent Number 6,066,528) provides teaching or suggestion of the features of the invention lacking in the combination of the APA, Kamiya, *et al.* ('624) and Kamiya, *et al.* ('615). That is, neither Ma, *et al.* nor Fazan, *et al.* teaches or suggests the features of the applicants' claimed slit-like common source line connected to source regions along a ground selection line pattern. Accordingly, combining either of Ma, *et al.* and Fazan, *et al.* with the APA, Kamiya, *et al.* ('624) and Kamiya, *et al.* ('615) does not result in teaching or suggesting the applicants' claimed invention. Accordingly, the claims are allowable over the cited references. Therefore, reconsideration of the rejections of claims 5 and 11 under 35 U.S.C. §103a based on Kamiya, *et al.* ('624), the APA, Kamiya, *et al.* ('615) and Ma, *et al.* or Fazan, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance.

Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774

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Steven M. Mills
Registration Number 36,610
Attorney for Applicants